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Invention: FORMATION OF ULTRA-THIN OXIDE LAYERS BY SELF-LIMITING INTERFACIAL OXIDATION

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SPECIFICATION

FORMATION OF ULTRA-THIN OXIDE LAYERS BY SELF-LIMITING INTERFACIAL OXIDATION

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor processing, and more particularly, to a method for forming uniform ultra-thin oxide layers.

BACKGROUND OF THE INVENTION

[0002] Thin oxide (e.g., SiO_2) and oxynitride (e.g., SiO_xN_y) layers are often used as dielectric layers at the Si surface of an integrated circuit. This is in part because of excellent electrical properties of the oxide and oxynitride layers, including high electron mobility and low electron trap densities. Semiconductor transistor technology is currently requiring oxide and oxynitride gate dielectric layers for conventional gate dielectric applications that are less than about 10-15 angstrom (A) thick, or as thin as 5-7 A for use as interface layers with high-dielectric constant materials (also referred to herein as high-k materials).

[0003] A native oxide layer that is typically a few angstrom thick, forms easily on clean Si surfaces, even at room temperature and atmospheric pressure. An oxide layer with a desired thickness that is larger than the native oxide thickness, can be grown through the native oxide layer, but usually the thickness uniformity and quality of the oxide layer is poor across the entire Si substrate.

[0004] Alternatively, the native oxide (or the chemical oxide) can be removed from Si surface prior to growing a new oxide layer. The native oxide layer can, for example, be removed using liquid baths containing dilute hydrofluoric acid (HF) or by using HF gas phase etching. A new oxide layer can then be re-grown on the clean Si surface by conventional thermal oxidation, but the initial oxidation can proceed quickly and result in poor thickness uniformity and inadequate electrical properties. For ultra-thin (<20 A) oxide layers used

in transistor technologies, the leakage current is dominated by the tunneling current.

SUMMARY OF THE INVENTION

[0005] A method is provided for forming ultra-thin oxide layers for gate dielectric applications, and other applications, such as dielectric interface layers underneath high-k materials. The method utilizes low processing pressure (and/or low partial pressure of an oxygen-containing gas) to achieve self-limiting oxidation of substrates that results in ultra-thin oxide layers.

[0006] In one embodiment of the invention, the substrates to be processed can be clean and lack an initial dielectric layer. Self-limiting oxidation of the substrates results in formation of ultra-thin oxide layers on the substrate.

[0007] In another embodiment of the invention, the substrates to be processed can contain an initial dielectric layer comprising at least one of an oxide layer, an oxynitride layer, a nitride layer, and a high-k layer. The initial dielectric layer is used to control the growth of ultra-thin oxide layers that are formed between the initial dielectric layer and the substrate in a self-limiting oxidation of the substrates.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] In the accompanying drawings:

[0009] FIG. 1A schematically shows a cross-sectional view of a gate electrode microstructure;

[0010] FIG. 1B schematically shows a cross-sectional view of an alternate gate electrode microstructure;

[0011] FIG. 2A schematically shows a cross-sectional view of a clean substrate;

[0012] FIG. 2B schematically shows a cross-sectional view of an oxide layer grown by a self-limiting process according to an embodiment of the present invention;

[0013] FIG. 3 shows a flowchart for forming an oxide layer according to an embodiment of the invention;

[0014] FIG. 4A schematically shows a cross-sectional view of a dielectric layer overlying a substrate;

[0015] FIG. 4B schematically shows a cross-sectional view of an oxide layer grown by a self-limiting process according to another embodiment of the invention;

[0016] FIG. 5A schematically shows a cross-sectional view of an oxide layer overlying a substrate;

[0017] FIG. 5B schematically shows a cross-sectional view of an oxide layer grown by a self-limiting process according to another embodiment of the invention;

[0018] FIG. 6 shows a flowchart for forming an oxide layer according to an another embodiment of the invention;

[0019] FIG. 7A shows oxide thickness versus oxidation time for oxide layers grown by a self-limiting process according to another embodiment of the present invention;

[0020] FIG. 7B shows oxide uniformity versus oxidation time for oxide layers grown by a self-limiting process according to another embodiment of the present invention; and

[0021] FIG. 8 shows a simplified block diagram of a processing system for forming oxide layers.

DETAILED DESCRIPTION OF THE INVENTION

[0022] A method is provided for forming ultra-thin oxide dielectric layers. These dielectric layers find use in semiconductor microstructures, for example, as gate dielectrics and as dielectric interface layers located between high-k materials and the underlying substrates. The method is capable of achieving ultra-thin layers, which can be of the order of few angstrom.

[0023] FIG. 1A schematically shows a cross-sectional view of a gate electrode microstructure. The gate electrode microstructure 10, which can be a part of an integrated circuit, comprises a substrate 100, a dielectric layer 102, and an electrode layer 106. The substrate 100 can, for example, be a Si substrate that is single-crystal Si or polycrystalline-Si (poly-Si). A Si substrate can include numerous active devices and/or isolation regions (not shown). A Si substrate 100 can be of n- or p-type, depending on the type of device being formed, and can, for example, consist of any diameter substrate, such as a

substrate with a diameter greater than about 195 mm, e.g., a 200 mm substrate, a 300 mm substrate, or an even larger substrate.

[0024] The dielectric layer 102 overlying the substrate 100 can, for example, be an ultra-thin (less than about 20 A) oxide layer. It should be noted that the term "oxide" includes oxidized materials containing oxygen that are typically used in semiconductor applications. Such materials include, for example, Si, that forms a SiO_2 dielectric layer upon oxidation. An oxide layer can be formed used thermal oxidation of the substrate in the presence of a process gas that includes an oxygen-containing gas, e.g., O_2.

[0025] Alternatively, the dielectric layer 102 can further contain at least one of an oxynitride layer, a nitride layer, and a high-k layer. Dielectric materials featuring a dielectric constant greater than that of SiO_2 (k~3.9) are commonly referred to as high-k materials. In addition, high-k materials may refer to dielectric materials that are deposited onto substrates rather than grown on the surface of the substrate (e.g., SiO_2, SiO_xN_y). The high-k layer can, for example, be selected from one of HfO_2, ZrO_2,Ta_2O_5, TiO_2, Al_2O_3, and HfSiO. In addition to the traditional doped poly-Si, the electrode layer 106 can, for example, comprise at least one of W, Al, TaN, TaSiN, HfN, HfSiN, TiN, TiSiN, Re, Ru, and SiGe.

[0026] In current semiconductor devices, one function of oxide gate dielectric layers is to "gate" the electrons, by controlling the flow of electricity across the transistor. With the introduction of high-k materials, these layers will likely still be required at the channel and/or gate electrode to preserve interface state characteristics. This includes forming an interface with good electrical properties, preventing uncontrolled Si surface oxidation, reducing reactions between different layers, and acting as a barrier layer to prevent diffusion of atoms to the different layers (e.g., dopant penetration from the gate electrode 106 into the substrate 100). In practice, good device performance depends on controlling the thickness of the dielectric layer 102, such that it remains thin, thereby avoiding increasing the equivalent oxide thickness (EOT) of the gate electrode structure.

[0027] FIG. 1B schematically shows a cross-sectional view of an alternate gate electrode microstructure. The gate electrode microstructure 20 in FIG. 1B differs from the gate electrode microstructure in FIG. 1A by a relatively

thick high-k layer 104 that is located between the electrode layer 106 and the dielectric layer 102. The high-k layer 104 in the gate electrode structure 20 can be physically thicker than the dielectric layer 102, while attaining the necessary capacitance

[0028] FIG. 2A schematically shows a cross-sectional view of a clean substrate. A clean substrate is a substrate that does not have an oxide layer. A substrate can be cleaned, for example, by placing it in a liquid bath containing dilute hydrofluoric acid (HF) or, alternatively, exposing it to HF gas phase etching. The dilute HF liquid solution can be a H_2O:HF (e.g., 50:1) mixture. Following the HF cleaning process, the substrate can be rinsed in de-ionized (D.I.) water prior to the oxidation process. A new ultra-thin oxide layer can be grown on the clean surface by a self-limiting process, where the oxide growth rate (and the resulting final oxide layer thickness) can be carefully controlled by selecting the appropriate process conditions, such as the partial pressure of the oxygen-containing gas in the process gas and in the process chamber, and the substrate temperature. FIG. 2B schematically shows a cross-sectional view of an oxide layer grown by a self-limiting process according to an embodiment of the present invention. The oxide layer 102B has a thickness D_{2B} that is uniform over the whole substrate 100.

[0029] Suitable process conditions that enable self-limiting growth of an oxide layer with a desired thickness and thickness uniformity can be determined by direct experimentation and/or design of experiments (DOE). For example, adjustable process parameters can comprise time, temperature (e.g., substrate temperature), process pressure, and composition of the process gas.

[0030] FIG. 3 shows a flowchart for forming an oxide layer according to an embodiment of the invention. At 200, the process is started. At 202, a substrate is positioned in a process chamber, and the chamber is evacuated. Following process chamber evacuation, organic contamination was effectively removed from the substrates at a process chamber temperature of about 300° C in an ambient containing about 1% oxygen. In addition, several pump/purge cycles were performed using an inert gas. At 204, a process gas including an oxygen-containing gas is flowed into the process chamber. The

partial pressure of the oxygen-containing gas can be less than about 50 Torr. Alternatively, the partial pressure of the oxygen containing gas can be less than about 40 Torr. The substrate temperature can be between about 500° C and about 1000° C, for example, about 700° C. The process chamber pressure can be lower than atmospheric pressure. In fact, the process chamber pressure can be lower than about 50 Torr. The thickness uniformity of the oxide layer can vary less than about 1 A over the substrate. At 206, an oxide layer with uniform thickness is formed on the substrate in a self-limiting oxidation process. The thickness of the oxide layer can be less than about 15 A. In fact, it can be less than about 10 A. The substrate is processed for a time period that enables formation of the desired oxide layer, and the process ends at step 208.

[0031] FIG. 4A schematically shows a cross-sectional view of a dielectric layer overlying a substrate. The initial dielectric layer 102C can, for example, comprise at least one of an oxide layer (e.g., SiO_2), a nitride layer (e.g., SiN), an oxynitride layer (e.g., SiO_xN_y), or a high-k layer, that can be deposited onto the Si substrate and is typically a few angstrom thick.

[0032] FIG. 4B schematically shows a cross-sectional view of an oxide layer grown by a self-limiting process process according to an alternate embodiment of the invention. The initial dielectric layer 102C in FIG. 4A is used to control the growth of an oxide layer 102D at the Si interface, where the thickness of the oxide layer 102D is controlled by a self-limiting oxidation of the Si substrate through the dielectric layer 102C. The initial dielectric layer 102C itself can be formed by a self-limiting oxidation process.

[0033] FIG. 5A schematically shows a cross-sectional view of an oxide layer overlying a substrate. The initial oxide layer 102E has a thickness D_{2E} and can, for example, consist of an ultra-thin native oxide layer that is typically a few angstrom thick, and forms easily on surfaces of various clean substrates (e.g., Si), even at room temperature and atmospheric pressure. Alternatively, the ultra-thin oxide layer can be a chemically deposited oxide layer. The initial oxide layer 102E can provide a starting oxide layer for growing a thicker oxide layer.

[0034] FIG. 5B schematically shows a cross-sectional view of an oxide layer grown by a self-limiting process in accordance with an alternate embodiment of the invention. The thickness D_{2E} of the oxide layer 102E in FIG. 5A is less than the thickness D_{2F} of the oxide layer 102F. Importantly, due to the self-limiting growth mechanism of the oxide layer 102F, it is not necessary for the initial oxide layer 102E to have good thickness uniformity, in order to grow an oxide layer 102F with good thickness uniformity.

[0035] FIG. 6 shows a flowchart for forming an oxide layer according to an alternate embodiment of the invention. At step 210, the process is started. At step 212, a substrate containing an initial dielectric layer is positioned in a process chamber and the chamber is evacuated. At step 214, a process gas comprising an oxygen-containing gas is flowed into the process chamber. At step 216 an oxide layer with uniform thickness is formed between the initial dielectric layer and the substrate in a self-limiting oxidation of the substrate. The substrate is processed for a time period that enables formation of the desired oxide layer, and the process ends at step 208. The process parameters can be as described above. Similar results were observed.

[0036] FIG. 7A shows oxide thickness versus oxidation time for oxide layers grown by a self-limiting process according to another embodiment of the present invention. Analogous to the oxide layer 102E overlying a substrate 100 shown in FIG. 5A, the starting 200mm Si substrates (wafers) in FIG. 7A, contained chemical oxide layers that were about 10A thick. Self-limiting oxidation of the Si substrates containing the chemical oxide layers was carried out for 3 to 80 min under low-pressure conditions. The oxidation process utilized a process gas containing an about 3:1 N_2:O_2 gas mixture, a process chamber pressure of about 8 Torr, and a substrate temperature of about 700°C. Typical gas flows were about 3 slm N_2 and about 1 slm O_2 in a batch type process chamber for a batch size of 100 wafers.

[0037] The oxidation curves in FIG. 7A show the average oxide thickness measured at 9 points (lower curve) and 49 points (upper curve) on the substrates using ellipsometry and a refraction index of 1.46. It is evident from FIG. 7A that the oxide growth saturates at an oxide thickness of about 15 A for these processing conditions. At each measured oxidation time (3, 10, 45,

80min), the oxide layer thickness varied by less than about 1 A for all 49 measurement points.

[0038] FIG. 7B shows oxide uniformity versus oxidation time for oxide layers grown by a self-limiting process according to another embodiment of the present invention. The oxide thickness uniformity for the 9 point and 49 point measurements is shown as %3-sigma values, and the overall trend shows improved oxide thickness uniformity over the whole Si substrate as the oxide layers grow thicker. Electrical measurements obtained for ultra-thin oxide layers (~15 A) shown in FIGs. 7A and 7B, showed good electrical properties when used as interface layers underneath high-k layers in gate electrode microstructures (see FIG.1B).

[0039] The basic mechanism in a dry oxidation process is the diffusion of an oxidizing species through an existing oxide layer and the reaction of the oxidizing species with the substrate at the oxide/substrate interface. In a self-limiting oxidation process, the rate of oxidation decreases as the thickness of the oxide layer increases. This is likely due to hindered diffusion of the oxidizing species through the existing oxide layer to the oxide/substrate interface. In order to achieve properties of self-limiting oxidation, the oxidation ambient forms an oxidation barrier on the substrate. In FIG. 7A, only about 0.5 A of additional oxide growth is observed during the last 30min of the 80min self-limited process, and the self-limiting process leads to a more uniform oxide layer thickness.

[0040] In the self-limiting oxidation process, shown in FIGs. 7A and 7B, it is observed that in substrate regions that contain a relatively thin oxide layer, an oxide layer grows faster than in regions where the oxide layer is thicker. This leads to formation of oxide layers where the thickness of the oxide layer is more uniform over the whole substrate, whether the initial oxide layer is uniform or not. We believe that the slow oxide growth rate that is observed in FIGs. 7A and 7B, permits long oxidation/anneal times, and improves the electrical quality of the resulting oxide layer, by removing bulk and interface traps, when a saturated, fully oxidized, stable oxide layer is formed.

[0041] In a self-limiting oxidation process, the oxide growth rate (and the resulting final oxide layer thickness) can be reduced/increased by decreasing/increasing the oxygen partial pressure in the process gas and in

the process chamber. In addition, the oxide growth rate can be reduced/increased by lowering/increasing the substrate temperature.

[0042] The oxidation data shown in FIGs. 7A and 7B, illustrates that it is possible to reproducibly grow oxide layers that are about 15 A thick, with excellent uniformity, from substrates containing oxide layers that are a few angstrom thick. The ability to start with substrates that contain an initial oxide layer (e.g., a chemical or native oxide), can remove the need to strip the initial oxide layer, prior to growing a new oxide layer on a clean substrate, as long as the initial oxide thickness is less than the desired final oxide thickness.

[0043] Semiconductor transistor technology is currently requiring oxide and oxynitride layers that are less than about 10-15 A thick for conventional gate dielectric applications (FIG. 1A), or as thin as about 5-7 A for use as dielectric interface layers with high-k materials (FIG. 1B). Formation of ultra-thin oxide layers that are thinner (<10A) than an initial oxide layer, can require removal of at least a portion of the initial oxide layer prior to growing thinner oxide layers.

[0044] In the aforementioned process example described in FIGs. 7A and 7B, the process gas comprised O_2 gas and N_2 inert gas. Alternatively, the inert gas can comprise at least one of Ar, He, Ne, Kr, Xe. The addition of an inert gas to the process chemistry is, for example, to dilute the process gas or adjust the process gas partial pressure(s). The parameter space for the oxidation process can, for example, utilize a chamber pressure less than about 50 Torr, a process gas flow rate less than about 2000 sccm, an inert gas flow rate less than about 1000 sccm, and a substrate temperature from about 500° C to about 1000° C. The substrate temperature can be held constant during the oxidation process or, alternatively, the substrate temperature can be ramped during the process.

[0045] A processing system for forming ultra-thin oxide layers can comprise a batch type process chamber capable of processing multiple substrates (wafers) simultaneously. Alternatively, the processing system can comprise a single wafer process chamber. The process chamber can process any diameter substrates, such as substrates with a diameter greater than about 195 mm, such as 200 mm substrates, 300 mm substrates, or even larger

substrates. A batch type process chamber can provide an advantage over single wafer process chambers by allowing long processing times for self-limiting processes

[0046] FIG. 8 shows a simplified block diagram of a processing system for forming oxide layers. The batch type processing system 300 comprises a process chamber 302, a gas injection system 304, a pumping system 306, a process monitoring system 308, and a controller 310. The gas injection system 304 is used to introduce a process gas for purging, cleaning, and processing the substrates 306. Multiple substrates 314 can be loaded into the process chamber 302 and processed using substrate holder 312. A self-limiting oxidation process that is carried out in a batch type processing system, can allow for a large number of tightly stacked substrates to be processed using substrate holder 312, thereby resulting in high wafer throughput.

[0047] When carrying out a self-limiting process, it can be advantageous to load the wafers to be processed into a process chamber 302 that is at a temperature below which wafer oxidation occurs. A typical process according to the invention comprised loading the wafers to be processed into a batch type process chamber that was at a temperature of about 300° C and comprised an ambient containing about 1% oxygen. These process conditions were effective in removing organic contamination from the substrates. In addition, several pump/purge cycles were performed using an inert gas.

[0048] Next, the process chamber temperature and process chamber pressure were adjusted to the desired values in an inert ambient to avoid substrate oxidation under non-equilibrium conditions. When the process temperature was reached, the substrates were exposed to a process gas for a time period that resulted in formation of the desired oxide layer. At the end of the oxidation process, the process chamber was evacuated and purged with an inert gas, and the substrates removed from the process chamber.

[0049] The process can be controlled by a controller 310 capable of generating control voltages sufficient to communicate and activate inputs of the processing system 300 as well as monitor outputs from the processing

system 300. Moreover, the controller 310 can be coupled to and exchange information with process chamber 302, gas injection system 304, process monitoring system 308, and a vacuum pumping system 306. For example, a program stored in the memory of the controller 310 can be utilized to control the aforementioned components of the processing system 300 according to a stored process recipe. One example of controller 310 is a DELL PRECISION WORKSTATION 610™, available from Dell Corporation, Dallas, Texas.

[0050] Real-time process monitoring can be carried out using process monitoring system 308 during processing. For example, mass spectroscopy (MS) can provide qualitative and quantitative analysis of the gaseous chemical species in the process environment. Process parameters that can be monitored using MS include gas flows, gas pressure, ratios of gaseous species, and gas purities. These parameters can be correlated with prior process results and various physical properties of the oxide or oxynitride layers.

[0051] It should be understood that various modifications and variations of the present invention may be employed in practicing the invention. It is therefore to be understood that, within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.